A Configurable OFDM Baseband Processor for RF-UOWC System-on-Chip

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***Abstract*—Dual-hop radio-frequency underwater optical wireless communication (RF-UOWC) systems enable underwater communication as well as above-water communication. RF technology is used for communication above the water surface, and optical communication is used underwater. In this work, we present an OFDM baseband processor on a programmable system-on-chip (SoC) FPGA. Our register transfer level (RTL) design of the OFDM is configurable, so it can be implemented for RF as well as UOWC. We have tested our design in real-time data transmission with both RF and underwater channels. The OFDM processor for RF communication is tested on ADRV9361-Z7035 FPGAs. With a channel bandwidth of 3.2 MHz, the achievable real-time data rate is 5.4 Mbps. The OFDM processor for UOWC is tested on RFSoC 4x2 FPGAs. With a channel bandwidth of 32 MHz, the achievable real-time data rate is 54 Mbps.**

I. Introduction

The Earth's surface is 70% covered with oceans, and the demand for underwater communication systems for marine exploration has been increasing. However, the traditional acoustic communication systems for underwater communication are limited by data rates, while RF wireless communication is heavily attenuated by sea water [1]. Underwater optical wireless communication (UOWC) is an emerging technology for underwater wireless communication. UOWC provides higher data rates than the traditional acoustic communication systems [2]. UOWC is also less attenuated by seawater compared to RF wireless communications.

In recent years, various UOWC experiments have been introduced [3], [4] aiming at increasing throughput beyond 10 Gbps. However, those experiments are still carried out in laboratory conditions with waveform generators and signal analyzers that have a sampling rate of up to 100 GS/s. More practical works in UOWC are also demonstrated in [5], [6], which use FPGAs. However, those experiments are still conducted at a throughput far below 1 Gbps due to the limited sampling speed of FPGAs compared to laboratory instruments. In our recent works [7], [8], [9], we have demonstrated free-space optical transmission using FPGAs that are also integrated with the Linux TCP/IP stack. We have elaborated on one of the hardware impairments from clock offset that can affect the performance of real-time optical OFDM transmission.

Recently, researchers also combined RF technology with UOWC into a dual-hop RF-UOWC system [10]. The communication above the water surface (first hop) is carried out using RF, while the communication underwater (second hop) is carried out using UOWC as illustrated in Fig. 1. There has been a lot of research in RF-UOWC in terms of security layers [11], [12], [13]. However, to the best of our knowledge, there are no reported works yet dealing with configurable OFDM baseband processor for RF-UOWC system-on-chip.

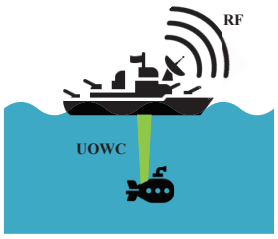

Fig. 1. An illustration of a hybrid RF-UOWC system. The above-water communication uses RF, while underwater communication uses UOWC.

Motivated by the above discussion, we consider designing a configurable OFDM baseband processor for the RF-UOWC system-on-chip. Our contributions are summarized as follows:

1) We designed a configurable OFDM baseband processor on FPGAs that can be used both for RF wireless communication and UOWC with minimal modification.
2) We evaluate the performance of the OFDM system in real-time TCP/IP transmission in the RF channel with the network and raw transmission in an underwater channel with a blue laser diode (LD) and photodiode (PD).

The remaining parts of this work are organized as follows. Section II describes the proposed system design. The experiment results are evaluated in Section III, followed by the conclusions in Section IV.

II. Proposed System Design

A. OFDM Processor Design

The most widely used OFDM in LED-based optical communication is intensity modulation/direct detection (IM/DD) that uses no carrier signal. In contrast, the OFDM for RF

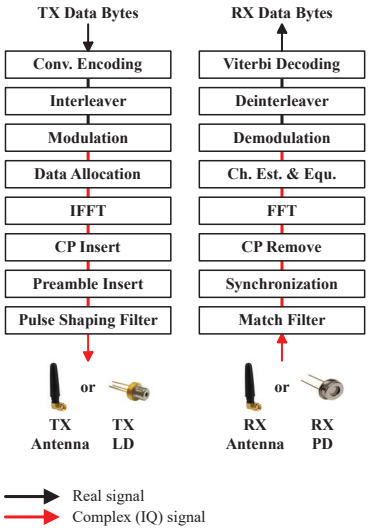

Fig. 2. Block diagram of the OFDM processor datapath.

TABLE I
LIST OF SUPPORTED MCS OF THE OFDM PROCESSOR.

MCS	Modulation	Rate
1	QPSK	1/2
2	16-QAM	1/2
3	QPSK	3/4
4	16-QAM	3/4

wireless systems is complex and bipolar. The Hermitian symmetry method is usually used to make LED-based OFDM produce real values only. However, the Hermitian method has a weakness, namely that the resulting channel bandwidth is reduced by half. Therefore, in order to achieve our goal of creating a configurable OFDM system for RF-UOWC, we consider using OFDM with a carrier signal for UOWC. As a result, the same OFDM design can be used both for RF and UOWC. This method is strandarized in the IEEE 802.11bb standard for light communication (LC) [14].

Fig. 2 shows our OFDM processor datapath block diagram. Our OFDM specification is based on the IEEE 802.16d standard. The transmitter (TX) datapath modulates TX data bytes into an OFDM frame. We implemented two types of encoding rates, namely 1/2 and 3/4, and we implemented two types of modulation, namely QPSK and 16-QAM. The modulation and coding (MCS) scheme that is used in our design is shown in Table I. Our OFDM symbol consists of 256 subcarriers consisting of 192 data points, 8 pilots, and 56 guards. On the receiver (RX) side, the datapath demodulates the OFDM frame to RX data bytes. We use synchronization to synchronize time and frequency. We use least squares channel estimation and the minimum mean squares (MMSE) equalizer. The input and output of the datapath are complex signals that will be further upconverted or downconverted before being connected to either an antenna or LD/PD.

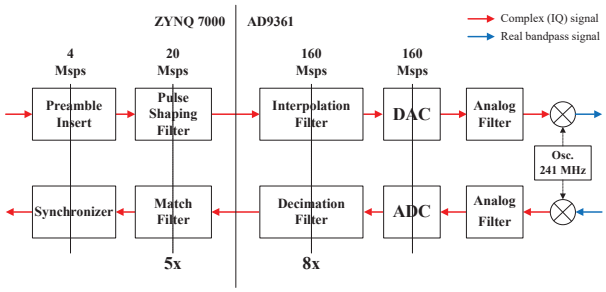

Fig. 3. ADRV9361-Z7035 digital-to-analog interface block diagram.

B. RF-UOWC System Configuration

There are two types of FPGA boards used in our work, namely ADRV9361-Z7035 for RF OFDM verification and RFSoC 4x2 for RF UOWC verification. The ADRV9361-Z7035 uses the Xilinx Zynq 7000 SoC chip, while the RFSoC 4x2 uses the Xilinx Zynq UltraScale+ RFSoC chip. The ADRV9361-Z7035 TX and RX paths support carrier frequencies from 70 MHz to 6.0 GHz, while the RFSoC 4x2 TX and RX paths support carrier frequencies from 0 to 6.0 GHz. We use a carrier frequency of 241 MHz for RF transmission and 49 MHz for UOWC transmission.

Fig. 3 shows the digital-to-analog system for the ADRV9361-Z7035 board. The signal bandwidth for the RF system is 3.2 MHz. We use a baseband clock frequency of 20 MHz. The pulse shaping filter on the TX interpolates the OFDM signal from 4 MSPS to 20 MSPS, and the match filter on the RX decimates the OFDM signal back from 20 MSPS to 4 MSPS. The interpolation filter on AD9361 interpolates the OFDM signal from 20 MSPS to 160 MSPS, and the decimation filter on AD9361 decimates the OFDM signal back from 160 MSPS to 20 MSPS. The sampling rate of the DAC and ADC is 160 MHz. The frequency cutoff of the AD9361's analog filter is set to 3.5 MHz. The carrier frequency is set to 241 MHz. On the RX path of the AD9361, there is an analog gain controller (AGC) with a maximum gain of 77 dB.

Fig. 4 shows the digital-to-analog system for the RFSoC 4x2 board. The signal bandwidth is 32 MHz. We use a baseband clock frequency of 200 MHz. The pulse shaping filter interpolates the OFDM signal to 200 MSPS, and the match filter decimates the OFDM signal back to 40 MSPS. The interpolation filter on RFDAC interpolates the OFDM signal to 3.2 GSPS, and the decimation filter on RFADC decimates the OFDM signal back to 200 MSPS. The sampling rate of the DAC and ADC is 3.2 GHz. The carrier frequency is set to 49 MHz. There are programmable numerically controlled oscillators (NCOs) and mixers inside the RFDAC and RFADC blocks that convert the baseband signal to the bandpass signal. However, on this FPGA board, there is no built-in AGC.

III. EXPERIMENT RESULTS

A. Hardware Resource

Table II shows the implementation results for the OFDM baseband processor. For the RF baseband processor, the syn-

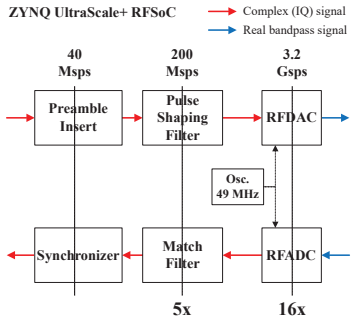

Fig. 4. RFSoC 4x2 digital-to-analog interface block diagram.

TABLE II
FPGA UTILIZATION OF THE OFDM PROCESSOR SOC.

Resource	RF System	UOWC System
LUT logic	28068	23894
LUT memory	1630	1652
FF	28416	25434
BRAM	93	60
DSP	51	51
Clock frequency	20 MHz	200 MHz
Power	0.873 W	0.776 W

thesis target is the Xilinx xc7z035ifbg676-2L device at an operating frequency of 20 MHz, while for the UOWC baseband processor, the synthesis target is the Xilinx xczu48dr-ffvg1517-2-e device at an operating frequency of 200 MHz. The result is that the RF system requires more resources compared to the UOWC system. This is justified due to the differences in the AXI interfaces and DAC/ADC interfaces used. The power consumption reported by the Xilinx tools for the RF system is 0.873 W, while for the UOWC system it is 0.776 W.

B. Experiment Setup

Fig. 5 shows our RF experiment setup. Two ADRV9361-Z7035 are used in the setup for TX and RX. We use 1/4 wave antennas that work at 241 MHz for downlink and 261 MHz for uplink. The distance between the boards is around 1.5 m. The host board is connected to a router that has an internet connection, while the client board is connected to the user's laptop via Ethernet. This RF setup is a full-duplex point-to-point system. The OFDM baseband processor is integrated into Linux's TCP/IP stack. Therefore, we can use real applications, such as `iperf`, to evaluate the system.

Fig. 6 shows our UOWC experiment setup. Two RFSoC 4x2 boards are used in the setup for TX and RX. For TX, we use Osram PL450B 450nm 80mW LD. This LD has a very high modulation bandwidth of approximately 1 GHz. We set the bias current for this LD to 30 mA by using a constant-current bench power supply. For RX, we use the Femto HSPR-X-I-1G4-SI ultra-high-speed Si-PIN PD module. This module has a bandwidth of 10 kHz to 1.4 GHz. The distance between TX and RX is 1.5 m. The boards are connected to the laptop via Ethernet and USB. This UOWC setup is a simplex system.

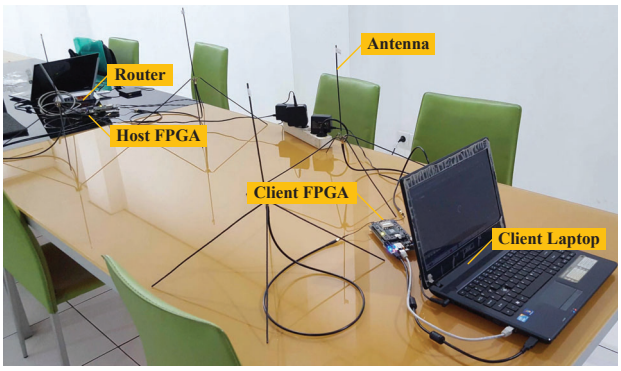

Fig. 5. Photograph of RF experiment setup with a 1/4 wave antenna at a distance of 1.5 m.

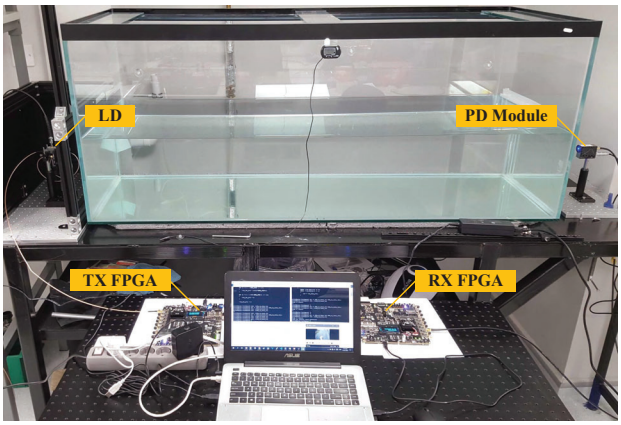

Fig. 6. Photograph of UOWC experiment setup with LD, PD, and a 1.5m water tank.

C. System Performance

We have tested the RF system without using any power amplifiers yet. The maximum output power from ADRV9361-Z7035 is 0 dBm. With this power, the maximum distance for error-free transmission is around 6 m for all MCS. The maximum real-time raw data rate is 5.4 Mbps, but after adding the Linux driver and TCP/IP stack, the maximum real-time data rate is 4.76 Mbps. Therefore, the overhead from the Linux driver and TCP/IP stack contributes to a 11.9% data rate penalty. The details of the RF system performance have been presented in [15].

We have tested the UOWC system by transmitting a video file. The video is RGB, and it has a size of 120x160 pixels. The video has a total of 120 frames. Therefore, the number of bits in the video file is 55296000. The maximum real-time data rate is 54 Mbps. The result is shown in Fig. 7. We also tested the UOWC system with turbulence. We added turbulence by adding a heater to the water tank. The scintillant index (SI) of the water is measured to be 0.188, while the normal condition without turbulence is 0.000322. The temperature of the water in the area of the heater is measured to be around 23°C, while the rest of the of the area is measured to be 21°C.

(a) (b)

Fig. 7. Screenshot of the video file after propagating through the underwater channel in (a) error-free condition and (b) non-error-free condition.

TABLE III
BER PERFORMANCE OF THE RF AND UOWC SYSTEMS.

MCS	RF BER	UOWC BER w/o turbulence	UOWC BER w/ turbulence
1	0	0	9.03e-03
2	0	3.52e-04	4.14e-02
3	0	0	3.01e-02
4	0	2.33e-03	1.57e-01

Table III shows the BER performance of the RF system, UOWC, without turbulence and with turbulence. The RF system produces a BER of 0. This can happen because the ADRV9361-Z7035 board has an AGC, which keeps the RX signal amplitude at the required limit. Meanwhile, in the UOWC system, which uses a RFSoC 4x2 board, there is no AGC. Therefore, this condition can affect the amplitude of the RX signal, which ultimately makes the BER worse. This can be seen in the UOWC system with the turbulence effect.

IV. CONCLUSIONS

In this work, we have designed a configurable OFDM baseband processor that can be used both for RF and UOWC systems. We have verified the system with the RF and UOWC channels. With a channel bandwidth of 3.2 MHz, the achievable real-time data rate is 5.4 Mbps. The OFDM design for UOWC communication is tested on RFSoC 4x2 FPGAs. With a channel bandwidth of 32 MHz, the achievable real-time data rate is 54 Mbps.

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